

EEE2007: Computer Systems and Microprocessors

Dr Rishad Shafik

Location: Merz Court, room E4.14

Telephone: (208)8155

Web: <http://www.ncl.ac.uk/eee/staff/profile/rishad.shafik>

E-mail: Rishad.Shafik@newcastle.ac.uk

Course outline

1. Microprocessor Architecture and Organisation (Hardware)

[Nick]

2. Computer Systems (System-level + Programming)

[Rishad]

- Systems: Memory, interconnects, processors
- Hardware: CPUs, GPUs, DSPs, and architectures
- Software: low-level and high-level C++ programming

www.rishadshafik.net/teaching.html

* References:

[Comp. Sys.] “Structured Computer Organization” - A. Tanenbaum, Prentice Hall.

[Program'g] “C++ How to Program” - Deitel, Pearson International 2005.

[misc.] See e-mail/blackboard for announcement(s).

[research] Energy-efficient and fault-tolerant systems, Rishad Shafik *et al*, Springer USA.

Lectures/Labs (Computer Systems)

- Monday 12noon-1pm and Tuesday 11am-1pm
 - (Stephenson Blg, F13)
 - Computer Systems theory and practice
- Tuesday 2pm-4pm
 - (Merz Court Computing Lab)
 - C++ based Computer Programming Theory + Demo + Lab
 - Lab Sessions: first Lab to be announced soon
- Tutorials and demonstrations
 - On demand

Lab/Projects/Exams

* This part will require lab and practical knowledge, too

Project 1, due on 15 Nov 2017 (data inference): 10% marks

Project 2, due on 13 Dec 2017 (machine learning): 10% marks

* Will contain theory lectures, coupled with practical sessions

(in the computing cluster/lab on floor 1)

- Will be complemented by demonstration sessions (when required)
- Exam: 30% (from RS part; including computing systems and programming)

Example References

- * Modern computing systems have evolved in complexities and applications

- * Hence, whenever opportunities arise – references and examples will be drawn from various processor and systems vendors
 - Arm: embedded systems
 - Intel: high-end computing systems
 - our very own developments in Microsystems
 - Coldfire: embedded and control systems (+ you know it well!)

- * These examples and reference will be used to complement your understandings

Discuss interests

If you are interested in

next-generation

intelligent

computing systems design (HW/SW)

aspects please feel free to discuss

If you blog or write for ICT matters in general – please feel free to contact.

Are you a freelance systems designer or contributor?

Group Discussions

- The course will require thinking through some aspects in groups
- Unfortunately you cannot always predict which group you would fall into
- This is to encourage peer discussions, this has often proved more effective than personal tutoring sessions to understand difficult aspects
- My job would be to facilitate this and ensure you get the most out of such discussions

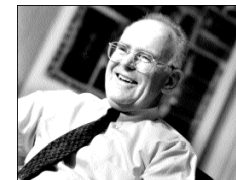
A group discussion primer

What is the future of computing?

What're your thoughts on the
future of computing?

Famous verses

- “I think there is a world market for maybe five computers.”
 - Thomas Watson, chairman of IBM, 1943.
- “There is no reason for any individual to have a computer in their home”
 - Ken Olson, president and founder of Digital Equipment Corporation, 1977.
- “640K [of memory] ought to be enough for anybody.”
 - Bill Gates, chairman of Microsoft, 1981.
- “...parallel computing will soon be relegated to the trash heap reserved for promising technologies that never quite make it.”
 - Ken Kennedy, CRPC Directory, 1994
- “Transistor density of semiconductor chips will increase by 2X every 18 months” – Gordon Moore, co-founder of Intel, 1965.

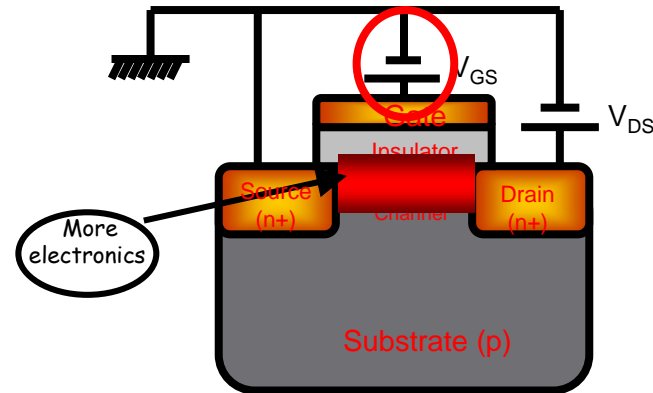
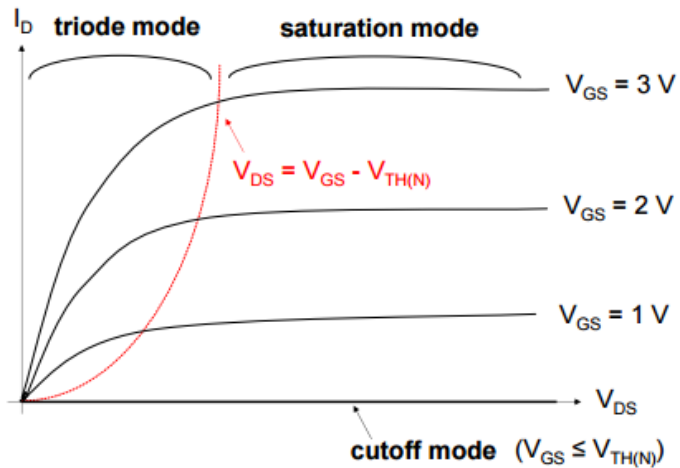
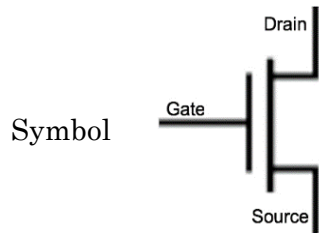


Computing is here to stay, the complexity and parallelisation will only rise with generations; it's important that we understand “every” bit of it as electronic engineers

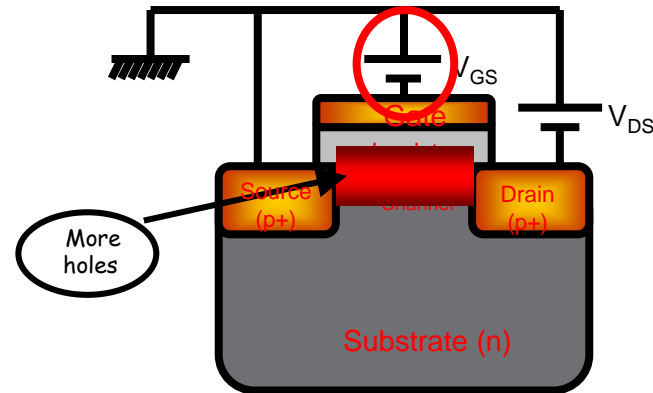
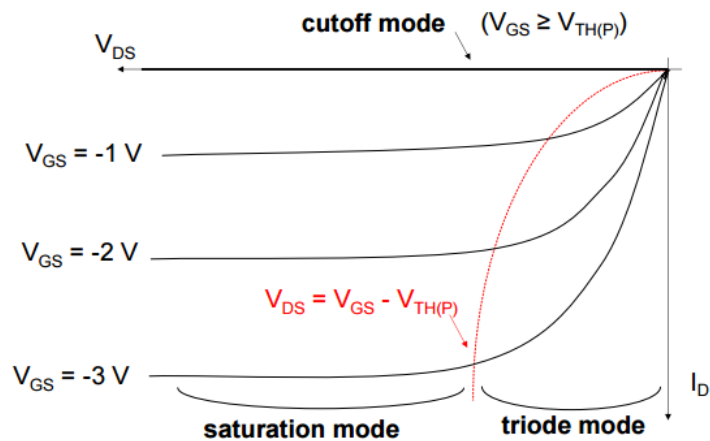
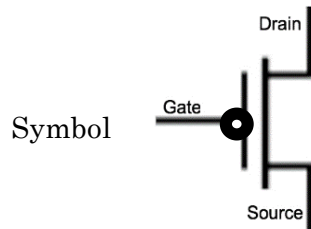


0.1: Background

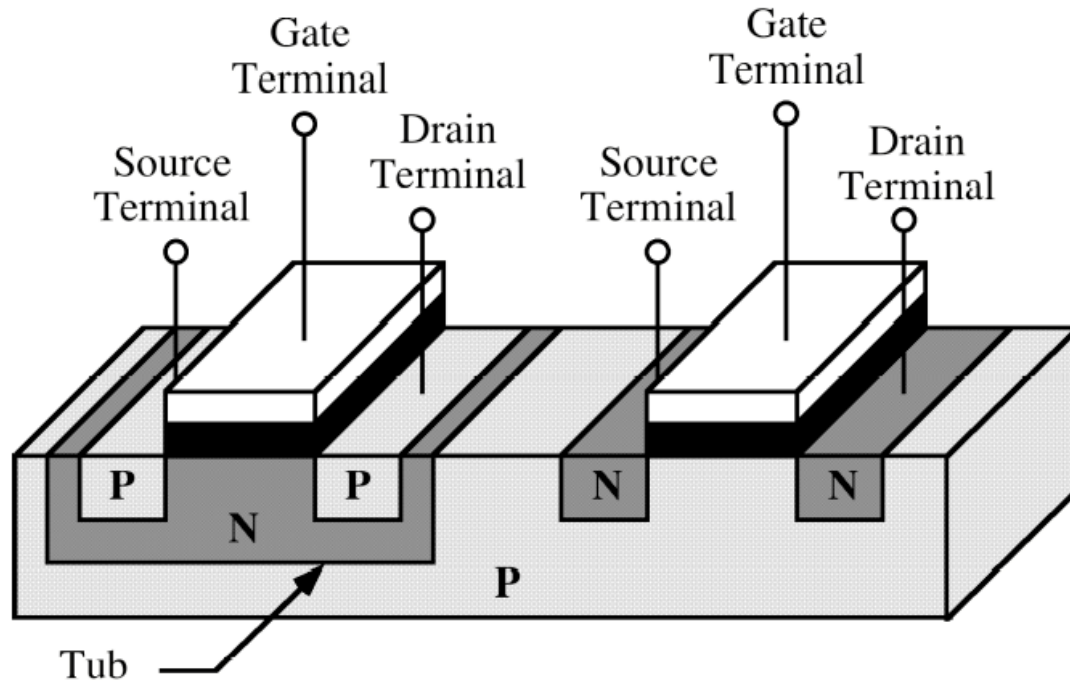
Transistor fundamentals: NMOS



Transistor fundamentals: PMOS



CMOS: complementary MOSFET

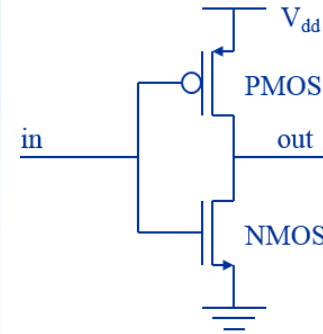


CMOS Logic Circuits: Inverter

- +ve supply at gate in will see NMOS shorted to ground
- -ve supply at gate in will see PMOS shorted to V_{dd}



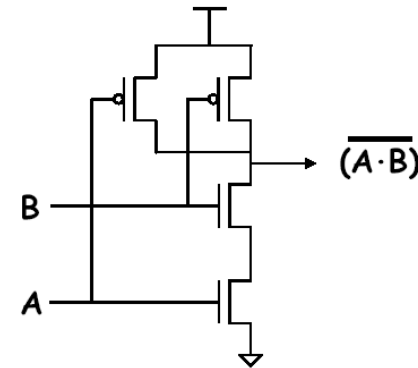
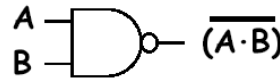
Symbol



Circuit

CMOS Logic Circuits: NAND

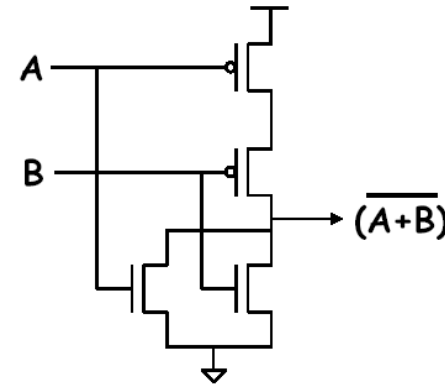
- +ve supply at A will see NMOS shorted to ground; PMOS open
- -ve supply at A will see PMOS shorted to Vdd, NMOS open
- +ve supply at B will see NMOS shorted; PMOS open
- -ve supply at B will see PMOS shorted to Vdd, NMOS open
- Now consider different A and B scenarios:
like A and B are both +ve



CMOS Logic Circuits: NOR

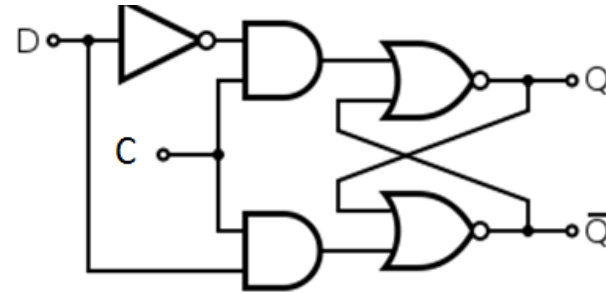
- +ve supply at A will see NMOS shorted to ground; PMOS open
- -ve supply at A will see PMOS shorted to Vdd, NMOS open
- +ve supply at B will see NMOS shorted to ground; PMOS open
- -ve supply at B will see PMOS shorted to Vdd, NMOS open

- Now consider different A and B scenarios:
like A and B are both -ve



D-type flip-flop (or Latches)

- Q outputs D input when Clock (C) is also positive
- Q_bar outputs D inverse when Clock (C) is also positive
- Clock and D drives the outputs
- The most basic sequential component



D	C	Q_{n+1}	
X	0	Q_n	Hold
0	1	0	Reset
1	1	1	Set

